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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/060,750	01/30/2002	Robert J. Devins	BUR9-2001-0016-US1	7058

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EXAMINER	
GUILL, RUSSELL L	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/060,750	DEVINS ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 and 8-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 8-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to a Request for Continued Examination filed May 21, 2008. Claims 2, 8 – 34 are pending. Claims 2, 8 – 34 have been examined. Claims 2, 8 – 34 have been rejected.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 21, 2008 has been entered.

Response to Remarks

3. Regarding claims 2 and 8 - 34 rejected under 35 USC § 112, second paragraph:

   a. Applicant's arguments have been fully considered, and are not persuasive.

   b. The Applicant argues:

   c. With respect to the rejection of independent claims 2, 8, and 15, and their dependent claims, Applicants currently amended these claims to more clearly describe a system comprising physical hardware. For example, currently amended claim 2 recites in part, "a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said design element in response to

signals produced by running a verification case", "a verification logic device connected to said SOC interface", and "wherein said verification logic device verifies said design element based on inputs from said first set of signals and said second set of signals". Independent claims 8 and 15, and those claims depending from independent claims 1, 8, and 15 are similarly amended in like manner.

d. With respect to the rejection of independent claims 21 and 28, and their dependent claims, Applicants currently amended these claims to more clearly describe a method directed to using physical hardware. For example, currently amended claim 21 recites in part, "producing a first set of signals and a second set of signals by a master central processing unit (CPU) of an SOC, which includes said design element, in response to running a verification case on said master CPU" and "inputting said first set of signals, received by said second EBIU, into said verification logic device; inputting said second set of signals, received by from said SOC interface, into said verification logic device; and verifying said design element based on inputs from said first set of signals and said second set of signals to said verification logic device". Independent claims 28 and those claims depending from independent claims 21 and 28 are similarly amended in like manner.

i. The Examiner respectfully replies:

ii. The specification appears to be directed to a software invention that is implemented in a computer. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Currently, the elements of the claim appear to have an interpretation as either physical hardware or a software model (*see especially paragraph [0025], and paragraphs [0001] – [0008]*).

iii. The specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001] – [0008]*), and does not

appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist.

e. The Applicant argues:

f. With respect to the phrase, "said verification test interface", lacking antecedent basis in claims 26 and 33, Applicants currently amended these claims to delete the phrase.

i. The Examiner respectfully replies:

ii. Applicant's argument is persuasive.

4. Regarding claims 2 and 8 - 34 rejected under 35 USC § 101:

a. Applicant's arguments have been fully considered, and are not persuasive, as discussed below.

b. The Applicant argues:

c. Claims 2, 8-14, 15-20, 21-27, and 28-34 stand rejected under 35 U.S.C. §101 because the Final Action asserts that the claimed invention is directed to non-statutory subject matter.

d. In particular, the Final Action asserts that regarding claims 2, 8-14, and 15-20, the claims are directed to a system for verification of a system-on-a-chip, but none of the claim limitations appear to expressly or inherently require tangible physical components. More particularly, the Final Action asserts that all of the claim components

appear to be software elements, including, the CPU, the SOC interface, and the EBIU interfaces (Final Action, page 5, section 7a).

e. In the currently amended claims above, Applicants respectfully aver that a CPU and an interface are, indeed, hardware. Newton's Telecom Dictionary, 20th edition, 2004 defines Central Processing Unit CPU as, "The part of a computer which performs the logic, computational and decision-making functions. It interprets and executes instructions as it receives them. Personal computers have one CPU, typically a single chip. It is the so-called 'computer on a chip.' That chip identifies them as an 8-bit, 16-bit or 32-bit machine." Likewise, Newton's Telecom Dictic nary, 20th edition, 2004 defines interface as, "1. A mechanical or electrical link connecting two or more pieces of equipment together."

i. The Examiner respectfully replies:

ii. While the Examiner appreciates the Applicant's arguments, the Examiner respectfully disagrees. The specification appears to be directed to a software invention that is implemented in a computer. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Currently, the elements of the claim appear to have an interpretation as either physical hardware or a software model.

f. The Applicant argues:

g. The Final Action also asserts that the independent claims do not appear to perform verification or produce a result that may be used in a practical application.

h. Applicants respectfully submit that the currently amended independent claims produce a practical result, i.e., "wherein said verification logic device verifies said design element based on

inputs from said first set of signals and said second set of signals", as recited in currently amended claims 1, 8, and[15, and "verifying said design element based on inputs from said first set of signals and said second set of signals to said verification logic device", as recited in currently amended claims 21 and 28.

i. The Examiner respectfully replies:

ii. The Examiner appreciates the Applicant's argument, but respectfully disagrees. The act of verification does not appear to produce a tangible result. The act of verification does not appear to produce an output that could be a tangible result. Accordingly, the rejection is maintained.

Claim Objections

5. Regarding claims 12 and 18, the claims recite, "verification test case". The Examiner respectfully requests the Applicant to ensure that the phrase is the intended phrase. The phrase, "said verification case" may be been intended.

6. Regarding claim 21, the claim recites in line 18, "by from". The phrase appears to be incorrect.

7. Regarding claim 26, the claim recites in lines 2 - 3, "said said". The phrase appears to be incorrect.

8. Regarding claim 26, the claim recites in line 4, "by from". The phrase appears to be incorrect.

9. Regarding claim 28, the claim recites in line 20, "by from". The phrase appears to be incorrect.

10. Regarding claim 33, the claim recites in lines 2 - 3, "said said". The phrase appears to be incorrect.

11. Regarding claim 33, the claim recites in lines 4 - 5, "by from". The phrase appears to be incorrect.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

13. Claims 2 and 8 - 34 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

a. Regarding claim 2 and dependent claims: claim 2 recites a CPU, an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware. The specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system (*see especially paragraph [0025], and paragraphs [0001] – [0008]*). The specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001] – [0008]*), and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004] - [0005] that appear to define

an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Further, the claim recites in line 13, "a verification logic device", which does not appear to have written description in the specification.

b. Regarding claim 8 and dependent claims: claim 8 recites a CPU, an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware. The specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system (*see especially paragraph [0025], and paragraphs [0001] – [0008]*). The specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001] – [0008]*), and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Further, the claim recites in line 14, "a verification logic device", which does not appear to have written description in the specification.

c. Regarding claim 15 and dependent claims: claim 15 recites a CPU, an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware. The specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system (*see especially paragraph [0025], and paragraphs [0001] – [0008]*). The specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001] – [0008]*), and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may

be in the form of a netlist. Further, the claim recites in line 14, "a verification logic device", which does not appear to have written description in the specification.

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

a. Claims 2, 8 – 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i. Regarding independent claims 2, 8 and 15, and dependent claims: the independent claims 2, 8 and 15 appear to be directed to a physical hardware system, however the specification appears to be directed to a software model of a physical hardware system (*Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist*). It is unclear whether the claims are directed to physical hardware or a software model. Any elements of the claims that are intended to be physical hardware should be clearly distinguished as physical hardware, and similarly, software elements should be distinguished.

ii. Regarding independent claims 21 and 28, and dependent claims: the independent claims appear to be directed to a method that uses physical hardware; however the specification appears to be directed to a software model of a physical hardware system (*Especially see the*

specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist). It is unclear whether the claims are directed to a method that uses physical hardware or a software model. Any elements of the claims that are intended to be physical hardware should be clearly distinguished as physical hardware, and similarly, software elements should be distinguished.

Claim Rejections - 35 USC § 101

15. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

16. Claims 2, 8 – 14, 15 – 20 and 21 – 27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. Regarding claims 2, 8 – 14, 15 - 20, the claims are directed to a system for verification of a design element of a system-on-chip, but none of the claim limitations appear to expressly or inherently require tangible physical components (*Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist*). An ordinary artisan interpreting the claim in light of the specification would reasonably interpret the claim as encompassing a purely software system. All of the components recited in the claim appear to have a reasonable interpretation as software elements, as discussed above, including the CPU, the SOC interface, and the EBIU interfaces. A claim that has both statutory

and non-statutory interpretations must be amended to have only statutory interpretations. Any elements of the claim that are intended to be physical hardware should be clearly distinguished as physical hardware. Further, since the system contains software, which is an abstract idea, the system must be directed to a practical application having a useful, concrete and tangible result.

b. Regarding claims 21 – 27, the claims are directed to a method that allows an interpretation of being software performed by a computer. A valid process under 35 USC § 101 must either 1) transform underlying subject matter, or 2) be tied to another statutory class, such as a particular apparatus. In order to qualify as a statutory process, the claim should positively recite the other statutory class to which it is tied, for example by identifying the apparatus that accomplishes the method steps. A mere recitation of a computer in the preamble does not appear to be sufficient to tie the process to a particular apparatus.

Allowable Subject Matter

17. Any indication of allowability is withheld pending resolution of the outstanding rejections.

Conclusion

18. The prior art made of record, and not relied upon, is considered pertinent to the applicant's disclosure:

a. Robert Devins, "SOC Verification Software - Test Operating System", April 2001, retrieved from the internet at http://www.eda-

stds.org/edps/edp01/PAPERS/devins.pdf, pages 185 - 190; teaches SOC verification wherein the SOC controls the testbench through a parallel channel.

19. The prior art made of record in a previous Office action, and not relied upon, is considered pertinent to the applicant's disclosure, and teaches common knowledge in the art:

a. M. Morris Mano, "Computer System Architecture", second edition, 1982, Prentice-Hall, pages 272, 433; appears to teach the essential architecture of the invention in figure 7-20.

b. Tom Shanley and Don Anderson, "ISA System Architecture", third edition, 1995, Addison-Wesley, pages 13, 16 - 19, 54, 125, 154, 241; teaches separate buses for address, data and control signals, and external bus interface units (figure 5-1).

c. Auerbach (U.S. Patent Number 6,199,126) teaches an EBIU on both ends of a bus (*figure 7*).

d. Nightingale (U.S. Patent Application Publication 2002/0183956) teaches SOC test software in an SOC controlling an external device.

e. Bergamaschi et al., "Designing systems-on-chip using cores", June 5, 2000, Proceedings of the 37th Design Automation Conference 2000, pages 420 - 425; teaches a slave device with a separate high-speed data bus and low-speed control bus connected to a SOC processor core (*figure 1, PLB Slaves, DCR bus, PLB Masters (e.g. CPU)*).

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:30 AM – 6:00 PM.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

/Paul L. Rodriguez/

Supervisory Patent Examiner,
Art Unit 2123